

WE CLAIM:

1. A method for forming a copper interconnect layer,
comprising:

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forming a first copper region over a semiconductor;

forming a low K dielectric layer over said copper
region;

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forming a plurality of vias in a first region of said
low K dielectric layer;

forming a trench with a first edge in said low K
15 dielectric layer over said plurality of vias wherein said
trench extends a minimum length X_{T0} beyond the edge α of a
via closest to the first edge of said trench; and
filling said trench and said plurality of vias with copper.

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2. The method of claim 1 wherein said trench is formed with
a first depth d_1 in said first region and a second depth d_2
at said trench edge wherein d_1 is greater than d_2 .

3. The method of claim 1 wherein said minimum length X_{T0} is
0.2um.

4. The method of claim 3 wherein said plurality of vias are
5 separated by a distance less than 1.0um.

5. An integrated circuit copper layer, comprising:

a low K dielectric layer over a semiconductor;

5 a plurality of vias in a first region of said low K dielectric layer;

a trench with a first edge in said low K dielectric layer over said plurality of vias wherein said trench
10 extends a minimum length X_{T0} beyond the edge α of a via closest to the first edge of said trench; and

a copper layer with a first edge in said trench and said plurality of vias wherein said first edge of said
15 copper layer coincides with said first edge of said trench and extends a minimum length X_{T0} beyond the edge α of said via closest to the first edge of said trench.

6. The integrated circuit layer of claim 5 wherein said
20 copper layer comprises a first thickness t_1 in said first region and a second thickness t_2 at said first edge wherein t_1 is greater than t_2 .

7. The integrated circuit copper layer of claim 5 wherein said minimum length X_{T0} is 0.2um.

8. The integrated circuit copper layer of claim 7 wherein
5 said plurality of vias are separated by a distance less than 1.0um.

9. A method for forming integrated circuit copper interconnects, comprising:

forming a first copper region over a semiconductor;

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forming a low K dielectric layer over said copper region;

forming a plurality of vias in a first region of said
10 low K dielectric layer wherein said plurality of vias are separated by a distance less than 1.0um;

forming a trench with a first edge in said low K dielectric layer with a first depth d_1 in said first region
15 and a second depth d_2 at said trench edge over said plurality of vias wherein d_1 is greater than d_2 , and said trench extends a minimum length of 0.2um beyond the edge α of a via closest to the first edge of said trench; and
20 filling said trench and said plurality of vias with copper wherein said copper used to fill said vias contacts said first copper region.